Am79C973
PCnet™-*FAST III*
Hardware User's Manual

AMD

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CHAPTER

1 INTRODUCTION

1.1 INTRODUCTION

The PCnet™-*FAST III* board is an advanced PC network interface adapter card targeted for the Fast Ethernet PCI adapter card market. It is based on the Am79C973 PCnet-*FAST III* device, a fully integrated 32-bit full-duplex, 10/100-Mbps Ethernet controller. Designed to address high performance system applications, the flexible bus master architecture provides high data throughput in the system and low CPU and system bus utilization. The PCnet-*FAST III* board supports the PCI Specification (Rev. 2.2), jumperless bus and media configuration, and driver software compatible with the existing PCnet family of drivers.

The PCnet-*FAST III* board fully supports ACPI/OnNow power management and AMD's Magic Packet™ technology. It also implements the de-facto standard 3-pin header for connecting the adapter to the power management circuitry of Magic Packet or Wake-on-LAN compliant system motherboard.

This manual provides a complete description of the PCnet-*FAST III* board, with sections covering the functional description of each building block, the setup and installation of the board, and the hardware specification.

It is assumed that the user of this manual has access to the information listed below, since references to these documents are made throughout this manual:

- *AMD Ethernet/IEEE 802.3 Family, 1994 World Network Data Book/Handbook (PID# 14287).*
- *Am79C973/Am79C975 PCnet-FAST III Single-Chip 10/100 Mbps PCI Ethernet Controller with Integrated PHY Preliminary Data Sheet (PID# 21510D)*
- *PCnet Family Network Driver Installation Guide (PID# 18233E)*
- *PCI Specification, Revision 2.2*

CHAPTER

2 FUNCTIONAL DESCRIPTION

2.1 BOARD DESCRIPTION

The PCnet-*FAST III* board is a 10/100-Mbps PCI network interface card. The Ethernet connection is implemented through the single RJ-45 jack which is connected to the internal 10/100 BASE-TX transceiver of the PCnet-*FAST III* device. Due to the high integration of the PCnet-*FAST III* device, very few external parts are needed. The PCnet-*FAST III* evaluation board provides the remote boot capability via an EPROM or a Flash device. The PCnet-*FAST III* evaluation card fully supports ACPI/OnNow power management including AMD's patented Magic Packet technology, through the LAN Wake-Up connector. This connector is used to supply standby power and carry the LAN Wake-Up signal. The connector is connected to the power management circuitry on the motherboard (if properly equipped).

The following diagram illustrates the implementation of the PCnet-*FAST III* board.

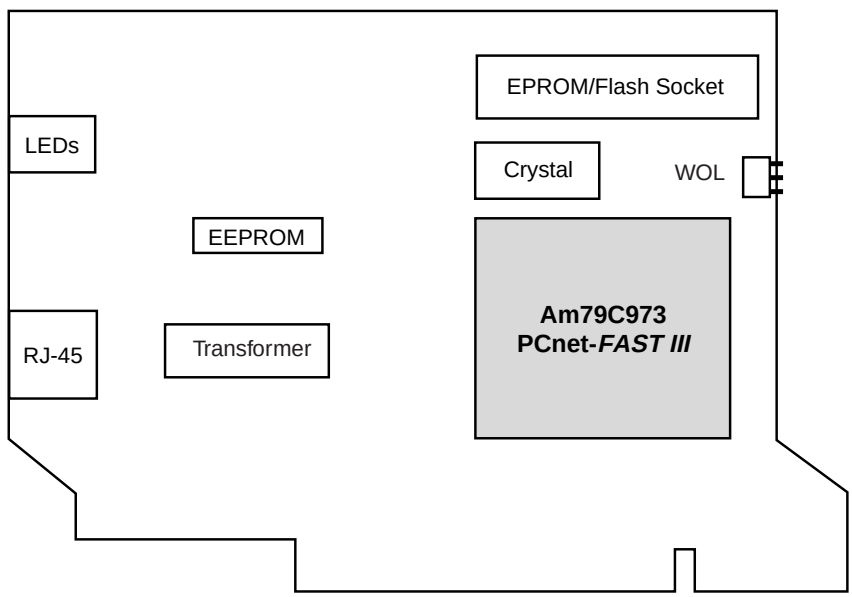


Figure 2-1 Board Diagram

2.2 ETHERNET NODE CONTROLLER

The Am79C973 PCnet-*FAST III* Ethernet controller is a fully integrated solution that contains a Bus Interface Unit (BIU), a DMA buffer management unit, an ISO/IEC 8802-3 and ANSI/IEEE 802.3-compliant 10/100 Mbps Media Access Control (MAC) and physical layer (PHY) function, a flexible buffer architecture with an SRAM-based FIFO extension for support up to 12 Kbytes of internal frame buffering, optional remote boot PROM/Flash, and advanced power management. The integrated PHY supports 10BASE-T, 100BASE-TX, and 100BASE-FX media interfaces.

2.3 LOCAL BUS INTERFACE

The PCnet-*FAST III* board implements the local bus interface to the Peripheral Components Interconnect (PCI) revision 2.2 specification through the Am79C973 chip. The BIU in the chip is designed to operate as a PCI bus master during normal operations, and some slave I/O accesses to the controller are required in normal operation as well. Initialization of the Ethernet controller is achieved through a combination of PCI Configuration Space accesses, bus slave accesses, bus master accesses, and an optional read of a serial EEPROM that is performed by the controller.

2.4 ETHERNET INTERFACE

The Ethernet interface for the PCnet-*FAST III* board is achieved through the single RJ-45 jack. The RJ-45 jack is connected through a transformer to the PCnet-*FAST III* controller. The transformer for the PCnet-*FAST III* device and board uses a 1:1.414 turns ratio for transmit (TX) and 1:1 turns ratio for receive (RX).

2.5 EXPANSION BOOT ROM/FLASH

The PCnet-*FAST III* board can accommodate up to 1 MByte of Boot ROM Code. An external latch is used to allow Boot ROM Address Latching for Boot ROM larger than 256 Kbytes. The PCnet-*FAST III* board supports EPROM or Flash as an Expansion boot ROM device. Both are configured using the same methods and operate the same way.

2.6 LAN WAKE-UP CONNECTOR

The LAN Wake-Up feature enables a system that is properly equipped to be awakened by a specially coded network packet. Receipt of a Magic Packet, or a network Wake-Up frame, or a change in Link status will awaken the system.

A LAN Wake-Up connector should be connected to the mother board with the special three-wire ribbon cable that is provided.

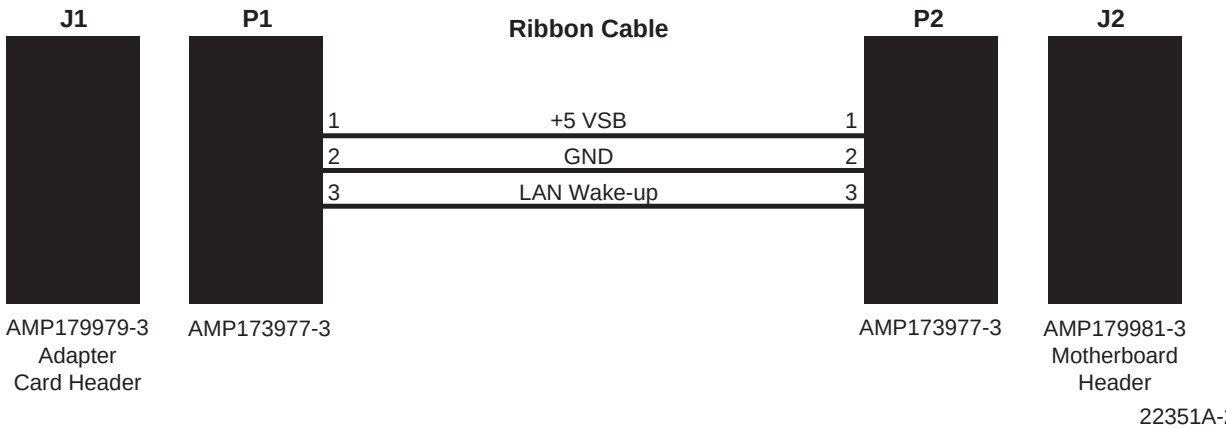


Figure 2-2 Ribbon Cable Definition and Recommended Connectors

2.7 LAN WAKE-UP THROUGH THE $\overline{\text{PME}}$ PIN

The PCnet-*FAST III* card also supports LAN Wake-Up by the $\overline{\text{PME}}$ pin. The PME pin and 3.3 V PCI auxiliary power (Vaux) are new additions to the PCI Specification, Revision 2.2. In systems where the $\overline{\text{PME}}$ pin is supported, LAN Wake-Up can be signaled by this pin. For systems that support the $\overline{\text{PME}}$ pin but do not have Vaux on the PCI bus/connector, the 3-pin LAN Wake-Up cable is still needed in order to provide auxiliary power (+5 VSB) to

the board. If Vaux is available, there is no need to use the LAN Wake-Up cable. In this case, the board will continually be powered through Vaux on the PCI bus in **all** power states.

2.8 SERIAL EEPROM INTERFACE

The PCnet-*FAST III* board stores the unique IEEE physical address and bus configuration of each node in the serial EEPROM. Once powered up, the Am79C973 chip automatically detects the presence of the EEPROM and reads the 41 words stored in it through the MicroWire interface protocol. For details of the MicroWire interface, refer to the Am79C973 data sheet. The interface also supports the WRITE operation to the EEPROM.

2.9 AUTO-NEGOTIATION CONTROL

The PCnet-*FAST III* board implements the Auto-Negotiation standard per the IEEE 802.3 specification. Auto-Negotiation automatically configures the link between two link partners through the Fast Link Pulse. The Fast Link Pulse is made up of a train of 17 clocks alternating with the 16 data fields for a total of 33 pulses. The two link partners send information in the 16 data positions between themselves. Both sides look to see what is possible and then connect at the greatest speed and capability (without any software support) as shown in the table below. The Auto-Negotiation capabilities for the PCnet-*FAST III* board are as follows:

Table 2-1 Auto-Negotiation Capabilities

Network Speed	Physical Network Type
200 Mbps	100BASE-TX, Full Duplex
100 Mbps	100BASE-TX, Half Duplex
20 Mbps	10BASE-T, Full Duplex
10 Mbps	10BASE-T, Half Duplex

If the Link partner is not able to Auto-Negotiate, the PCnet-*FAST III* card parallel detects the other side. This means it detects the speed correctly, but it cannot ascertain the duplex mode and reverts to Half-Duplex mode.

2.10 CRYSTAL INFORMATION

The PCnet-*FAST III* board uses a 25-MHz fundamental type, parallel resonant crystal with 50-100 ppm accuracy and 18 pF of capacitive load.

2.11 MAGNETICS INFORMATION

The PCnet-*Fast III* board requires a transformer with a turns ratio of 1:1.414 (device:cable) on transmit and 1:1 on receive. Table 2-2 provides an approved vendor list of magnetics recommended for use with the PCnet-FAST III device.

Table 2-2 Recommended Magnetics Vendors

Vendor	Part Number	Package
Halo	TG22-SI43ND	16-pin module
Halo	TG22-SI41N2	16-pin module
Halo	TG110-SI41N2	16-pin module
Bel Fuse	S558-5999-G9	16-pin module
Bel Fuse	S558-5999-G8	16-pin module
Pulse Engineering	H1081	16-pin module
Pulse Engineering	H1119	16-pin module
PCA Electronics	EPF8095G	16-pin module
PCA Electronics	EPF8096G	16-pin module

CHAPTER

3 SETUP AND INSTALLATION

3.1 BOARD CONFIGURATION

Configuration of the I/O base address and the interrupt channel is automatic upon power up, without any hardware jumpers. The system BIOS routine is responsible for assigning the I/O base address and binding the appropriate interrupt channels to the PCnet-*FAST III* board.

3.2 10/100BASE-T PHYSICAL CONNECTIONS

A Data Terminal Equipment (DTE) system with the installed PCnet-*FAST III* board can connect to an Ethernet network using the on-board RJ-45 jack for either 10BASE-T or 100BASE-TX connection. Figure 3-1 illustrates a typical network configuration for the network using the PCnet-*FAST III* board.

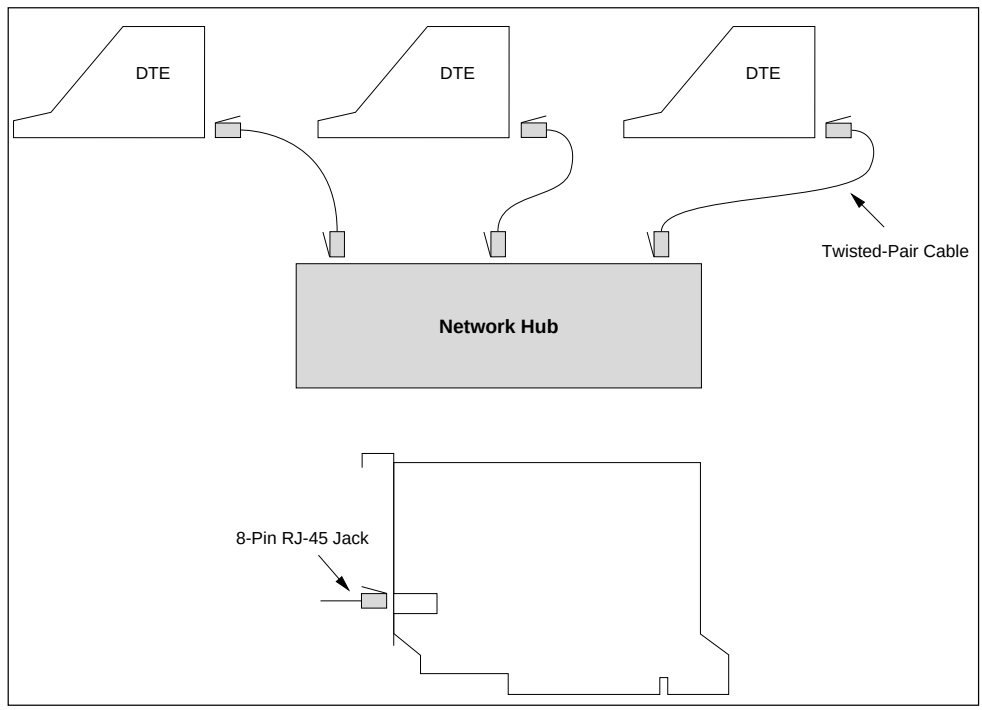


Figure 3-1 10/100BASE-T Physical Connections

The Auto-Negotiation feature of the PCnet-*FAST III* controller configures whether the capability of the network is 10 Mbps or 100 Mbps, and whether it is full or half-duplex. See Auto-Negotiation Control, section 2.9.

3.3 NETWORK STATUS

Four LEDs on the bracket provide the network status as shown in the following table:

LED	LED 0	LED 1	LED 2	LED 3
Color	Green	Green	Amber	Green
Function	LNKST	ACT	10/100 (*Note 1*)	COL/MP (*Note 2*)
Meaning	On = Link Pass Off = Link Fail	On = Receive or Transmit Off = No Activity	On = 100 Mbps Off = 10 Mbps	On = Collision or Magic Packet Off = No Collision

Notes:

1. Valid only when LED 0 is On.

2. When adapter is powered up and in operating mode, LED 3 indicates a collision. When adapter is powered down or in low-power state, LED 3 indicates that the controller is in Magic Packet mode and is ready to receive a network Wake-Up frame.

The placement of the LEDs are shown in Figure 3-2.

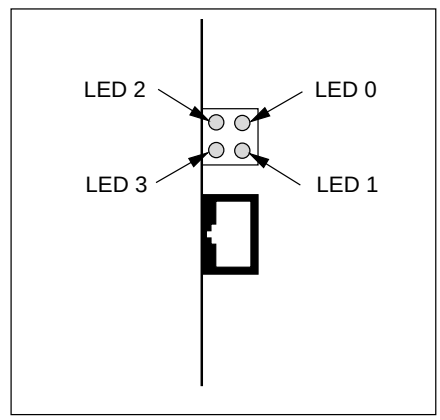


Figure 3-2 LED Placement

CHAPTER

4 HARDWARE SPECIFICATIONS

4.1 PCI INTERFACE

The Am79C973 chip on the PCnet-*FAST III* board contains the interface logic to the PCI bus. Connections to the PCI bus are straightforward in that there is no external glue logic on the PCnet-*FAST III* board, thus making the PCnet-*FAST III* board fully compliant to the PCI loading and trace length specifications.

The types of PCI cycles supported on the PCnet-*FAST III* board are as follows:

- Master Memory Read
- Master Memory Write
- Master Memory Read Line
- Master Memory Read Multiple
- Slave Configuration Read
- Slave Configuration Write
- Slave I/O Read
- Slave I/O Write

The first three types are the Master cycles that the Am79C973 chip uses to transfer data across the PCI bus. The Am79C973 chip owns and controls the address/data bus after its request is acknowledged by the system arbiter. If there are two or less double words to read, the Am79C973 chip uses the Memory Read cycle; if there are more than two double words to read, the Am79C973 chip uses the Memory Read Line cycle. All Master cycles also support the four types of slave termination schemes specified in the PCI Revision 2.2 specification.

The last four types are the Slave cycles that the host CPU uses to access configuration and register information in the Am79C973 chip.

4.2 I/O BASE ADDRESS AND INTERRUPT

In a PCI system, the I/O base address and the interrupt channel that the PCnet-*FAST III* board uses are assigned by the POST routine. Software drivers determine the I/O base address and the interrupt channel assigned to the PCnet-*FAST III* board by reading the PCI configuration space of the device.

Table 4-1 I/O Port Address

I/O Resource	Access Code
APROM	I/O Base address + 0h
RDP	I/O Base address + 10h
RAP	I/O Base address + 12h for word I/O mode (in Am1500 driver compatible mode)
	I/O Base address + 14h for double word mode
Reset Register	I/O Base address + 14h for word I/O mode (in Am1500 driver compatible mode)
	I/O Base address + 1Ch for double word I/O mode
BDP	I/O Base adddres + 16h for word I/O mode (in Am1500 driver compatible mode)
	I/O Base address +1Ch for double word I/O mode

4.3 RJ-45 INTERFACE

The PCnet-*FAST III* board is equipped with a RJ-45 type, eight-pin modular interface. The pin configuration and definition for the RJ-45 connection are as follows:

Table 4-2 RJ-45 Pinout

Pin Number	Color Code	Function
Pin 1	white/orange band	TX+
Pin 2	orange/white band	TX-
Pin 3	white/green band	RX+
Pin 6	green/white band	RX-
Pin 4	blue/white band	Not Used
Pin 5	white/blue band	Not Used
Pin 7	solid orange	Not Used
Pin 8	solid gray	Not Used

The color code may vary from one cable manufacturer to another. Make sure that the TX+ and the TX- wires are twisted as a pair and the RX+ and the RX- wires are twisted as another pair. For 100-Mbps operation, category 5 wire must be used for proper 100BASE-TX operation.

Note: *Do not use the telephone-type cable commonly known as "silver satin" (flat, with silver vinyl jacket) to connect the stations as none of the wires are twisted.*

4.4 SERIAL EEPROM

The serial EEPROM contains the IEEE physical address unique to each node, the bus configuration, and the MAU configuration information. The format of the EEPROM contents is the following, beginning with the byte that resides at the lowest EEPROM address.

Table 4-3 Am79C973 EEPROM Map

Word Address	Byte Addr	Most Significant Byte	Byte Addr	Least Significant Byte
00h*	01h	2nd byte of the ISO 8802-3 (IEEE/ANSI 802.3) station physical address for this node	00h	First byte of the IS0 8802-3 (IEEE/ANSI 802.3) station physical address for this node, where “first byte” refers to the first byte to appear on the 802.3 medium
01h	03h	4th byte of the node address	02h	3rd byte of the node address
02h	05h	6th byte of the node address	04h	5th byte of the node address
03h	07h	CSR116[15:8] (OnNow Misc. Config).	06h	CSR116[7:0] (OnNow Misc. Config.)
04h	09h	Hardware ID: must be 11h if compatibility to AMD drivers is desired	08h	Reserved location: must be 00h
05h	0Bh	User programmable space	0Ah	User programmable space
06h	0Dh	MSB of two-byte checksum, which is the sum of bytes 00h-0Bh and bytes 0Eh and 0Fh	0Ch	LSB of two-byte checksum, which is the sum of bytes 00h-0Bh and bytes 0Eh and 0Fh
07h	0Fh	Must be ASCII “W” (57h) if compatibility to AMD driver software is desired	0Eh	Must be ASCII “W” (57h) if compatibility to AMD driver software is desired
08h	11h	BCR2[15:8] (Miscellaneous Configuration)	10h	BCR2[7:0] (Miscellaneous Configuration)
09h	13h	BCR4[15:8] (Link Status LED)	12h	BCR4[7:0] (Link Status LED)
0Ah	15h	BCR5[15:8] (LED1 Status)	14h	BCR5[7:0] (LED1 Status)
0Bh	17h	BCR6[15:8] (LED2 Status)	16h	BCR6[7:0] (LED2 Status)
0Ch	19h	BCR7[15:8] (LED3 Status)	18h	BCR7[7:0] (LED3 Status)
0Dh	1Bh	BCR9[15:8] (Full-Duplex control)	1Ah	BCR9[7:0] (Full-Duplex Control)
0Eh	1Dh	BCR18[15:8] (Burst and Bus Control)	1Ch	BCR18[7:0] (Burst and Bus Control)
0Fh	1Fh	BCR22[15:8] (PCI Latency)	1Eh	BCR22[7:0] (PCI Latency)
10h	21h	BCR23[15:8] (PCI Subsystem Vendor ID)	20h	BCR23[7:0] (PCI Subsystem Vendor ID)
11h	23h	BCR24[15:8] (PCI Subsystem ID)	22h	BCR24[7:0] (PCI Subsystem ID)
12h	25h	BCR25[15:8] (SRAM Size)	24h	BCR25[7:0] (SRAM Size)
13h	27h	BCR26[15:8] (SRAM Boundary)	26h	BCR26[7:0] (SRAM Boundary)
14h	29h	BCR27[15:8] (SRAM Interface Control)	28h	BCR27[7:0] (SRAM Interface Control)
15h	2Bh	BCR32[15:8] (MII Control and Status)	2Ah	BCR32[7:0] (MII Control and Status)
16h	2Dh	BCR33[15:8] (MII Address)	2Ch	BCR33[7:0] (MII Address)
17h	2Fh	BCR35[15:8] (PCI Vendor ID)	2Eh	BCR35[7:0] (PCI Vendor ID)
18h	31h	BCR36[15:8] (Conf. Space. byte 43h alias)	30h	BCR36[7:0] (Conf. Space byte 42h alias)
19h	33h	BCR37[15:8] (DATA_SCALE alias 0)	32h	BCR37[7:0] (Conf. Space byte 47h0alias)
1Ah	35h	BCR38[15:8] (DATA_SCALE alias 1)	34h	BCR38[7:0] (Conf. Space byte 47h1alias)
1Bh	37h	BCR39[15:8] (DATA_SCALE alias 2)	36h	BCR39[7:0] (Conf. Space byte 47h2alias)
1Ch	39h	BCR40[15:8] (DATA_SCALE alias 3)	38h	BCR40[7:0] (Conf. Space byte 47h3alias)
1Dh	3Bh	BCR41[15:8] (DATA_SCALE alias 4)	3Ah	BCR41[7:0] (Conf. Space byte 47h4alias)
1Eh	3Dh	BCR42[15:8] (DATA_SCALE alias 0)	3Ch	BCR42[7:0] (Conf. Space byte 47h5alias)
1Fh	3Fh	BCR43[15:8] (DATA_SCALE alias 0)	3Eh	BCR43[7:0] (Conf. Space byte 47h6alias)
20h	41h	BCR44[15:8] (DATA_SCALE alias 0)	40h	BCR44[7:0] (Conf. Space byte 47h7alias)
21h	43h	BCR48[15:8]Reserved location:must be 00h	42h	BCR48[7:0]Reserved location: must be 00h
22h	45h	BCR49[15:8]Reserved location:must be 00h	44h	BCR49[7:0]Reserved location: must be 00h
23h	47h	BCR50[15:8]Reserved location:must be 00h	46h	BCR50[7:0]Reserved location: must be 00h
24h	49h	BCR51[15:8]Reserved location:must be 00h	48h	BCR51[7:0]Reserved location: must be 00h
25h	4Bh	BCR52[15:8]Reserved location:must be 00h	4Ah	BCR52[7:0]Reserved location: must be 00h
26h	4Dh	BCR53[15:8]Reserved location:must be 00h	4Ch	BCR53[7:0]Reserved location: must be 00h
27h	4Fh	BCR54[15:8]Reserved location:must be 00h	4Eh	BCR54[7:0]Reserved location: must be 00h
28h	51h	Checksum adjust byte for the 82 bytes of the EEPROM contents, checksum of the 82 bytes of the EEPROM should total to FFh	50h	BCR55[7:0]Reserved location: must be 00h
Empty locations – Ignored by device				
3Eh	7Dh	Reserved for Boot ROM usage	7Ch	Reserved for Boot ROM usage
3Fh	7Fh	Reserved for Boot ROM usage	7Eh	Reserved for Boot ROM usage

Note: **Lowest EEPROM address.*

The IEEE physical address is unique to each node and manufacturer. Each manufacturer of the PCnet-*FAST III* board must only use the address block assigned to their company. AMD uses *00 00 1A 18 XX XX address block.* To apply for an IEEE block address, the board manufacturer must contact:

IEEE Standard Department
445 Hoer Lane
Piscataway, NJ 08855-1331
c/o OUI Registrar
Tel: (908) 562-3809

The EEPROM contents could either be pre-programmed on an off-line EEPROM programmer, or be programmed on the PCnet-*FAST III* board via the MicroWire protocol. The actual programming procedure on the off-line is left to the user.

Note: *The last four digits of the IEEE address can be found on a label attached to the EEPROM of the PCnet-FAST III board.*

4.5 PHYSICAL DIMENSIONS

Without the bracket mounted to the board, the physical dimensions of the board are as follows:

- Width: 4.4 inches
- Height: 3.2 inches

4.6 POWER REQUIREMENTS

The power requirement of this board is 750 mW maximum at 3.3 V DC and 25° C.

To properly reflect the power consumption of the board in the PCI environment, the PRSNT#1 and PRSNT#2 signals on the boards are shorted to Ground according to the PCI rev 2.2 Specification.